

Method for manufacturing multi-chip package having encapsulated bonding wires between stack chips

Publication number: TW250597B

Publication date: 2006-03-01

Inventor: LIN CHUNG-HUNG (TW); CHOU SHIH-WEN (TW); PAN YU-TANG (TW); SU MING-HUNG (TW)

Applicant: CHIPMOS TECHNOLOGIES INC (TW); CHIPMOS TECHNOLOGIES BERMUDA (BM)

Classification:

- **International:** (IPC1-7): H01L21/60

- **European:**

Application number: TW20040141901 20041231

Priority number(s): TW20040141901 20041231

Report a data error here

Abstract of TW250597B

A method for multi-chip package is disclosed. A first chip is disposed on a chip carrier. A first chip adhesive layer is formed on an active surface of the first chip and exposes pads on the first chip. Then, a wire-bonding step is processed to electrically connect the pads on the first chip to the chip carrier through a plurality of first bonding wires. At least a second chip is provided with a second chip adhesive layer formed on backside of the second chip in wafer form. Utilizing picking and placing, the second chip is stacked on the first chip adhesive layer, and the second chip adhesive layer is combined with the first chip adhesive layer to seal portions of the first bonding wires above the active surface of the first chip. It could package a plurality of central pads chip and protect the first bonding wires.

Data supplied from the esp@cenet database - Worldwide